REMARKS

Claims 1-17 are currently pending. Claims 1, 7, and 13-17 have been amended for clarification. The title has been amended to correct for a typographical error. It is respectfully submitted that no new matter has been added.

The Patent Office provisionally rejected claims 1-17 under 35 U.S.C. 101 as claiming the same invention as that of claims 1-17 of copending Application No. 10/740,036.

The Patent Office asserted on page 3, line 8, of the Office Action dated October 26 2007 "The conflicting claims are identical."

Applicant has disclosed, on page 6, line 30, through page 7, line 2, as follows: "In accordance with an aspect of this invention, the Tier-2 Scheduler 92 uses the inherited priority from the application 30, as obtained from the OS Scheduler 45, to determine the optimal scheduling of the algorithm logics in the DCHL 50."

All claims of the current patent application recite "with inherited application priorities," subject matter that is not recited in any of the claims in copending Application No. 10/740,036.

Thus, there is no double patenting. The Patent Office is respectfully requested to withdraw its rejection of claims 1-17 under 35 U.S.C. 101.

The Patent Office asserted on page 3, lines 1-4, of the Office Action dated October 26 2007 that claims 1-6 and 13-17 were rejected under 35 U.S.C. 101 as they appeared to be comprised of software alone and that the claims are not supported by either a specific and substantial asserted utility or a well established utility. With the amendment of claims 1 and 13, it is believed that the rejection under 35 U.S.C. 101 has been overcome.

The Patent Office rejected claims 1-17 under 35 U.S.C. 112, second paragraph, as indefinite.

As to claim 1, Dynamic Configurable Hardware Logic (DCHL) and TiEred Multimedia Acceleration Scheduler (TEMAS) are both described with definiteness in the current application, as described below.

DCHL is hardware described on page 4, line 23, through page 5, line 4, as follows:

> the basic unit of the DCHL architecture is the Logic Element (LE) 10, a plurality of which are arranged in a context plane 12, or more simply a context. A plurality of context planes 12 result in a multi-context 14. The LE 10 is a unit to be configured as an algorithm logic, and an algorithm

> logic is assumed to include a set of LEs 10. More than one context 12 can be included in a single device, and more than one algorithm logic can be configured into one context 12, and can operate simultaneously.

TiEred Multi-media Acceleration Scheduler is described on page 5, lines 19-21, as follows:

> a multi-layered scheduler, such as a two-layered scheduler, is referred to as a TiEred Multi-media Acceleration Scheduler (hereinafter TEMAS) which deals with the DCHL layer as a generic system software model.

Applicant believes that both DCHL and TEMAS have been described with sufficiently definiteness in the application. The claims are read in the context of the application, and therefore are seen to meet the definiteness requirement of 35 U.S.C. 112, second paragraph.

As to claim 2, a description of the Tier-1 scheduler and the Tier-2 scheduler is found on page 5, line 19, through page 6, line 11, as follows:

> a multi-layered scheduler, such as a two-layered scheduler, is referred to as a TiEred Multi-media Acceleration Scheduler (hereinafter TEMAS) which deals with the DCHL layer as a generic system software model. Referring to FIG. 4A, four typical device layers are shown: the application layer 60 (containing three exemplary applications 30A, 30B, 30C), a service layer 80, a node layer 90 and the hardware layer 70 (the DCHL 50 layer). The Tier-1 Scheduler 82, containing a scheduling algorithm 82A, is shown resident at the service layer 80, while a plurality of Tier-2 Schedulers 92, 94, 96 are resident at the node layer 90, one for each node entity 90A. An OS Scheduler 45, part of the OS 40, is shown resident in the service layer 80 with the Tier-1 Scheduler 82. The OS Scheduler 45 manages all applications 30 that are ordinary applications, and multi-media applications that use the DCHL 50. The Tier-1 Scheduler 82 obtains scheduling information about multi-media applications from the OS Scheduler 45, via a Hook Module 47 (shown in FIG. 4B). The most important information is the scheduling order of applications 30 and the priorities (see (a) in FIGS. 4B and 9). The scheduling order is used to decide when preloading is performed for the DCHL 50. The priority of the applications gives the actual priority of the algorithm logic to be configured into and executed on the DCHL 50 (see FIG. 5). Since the priority of the algorithm logic cannot be determined until an actual application is attached to it, this function of the Tier-1 Scheduler 82 is important (see scheduling of events (b) and (c) in FIGS. 4B and 9). The Tier-1 Scheduler 82 also obtains communication overhead from the device driver, and determines the difference in timing for the DCHL

hardware (see (d) in FIG. 4B), which aids in adjusting the scheduling timing.

A Tier-1 Scheduler 82 and Tier-2 Schedulers 92, 94, 96 are shown in Figure 4A.

Applicant submits that Tier-1 and Tier-2 schedulers are clearly disclosed in the application as filed.

As to claim 4, it is clear that context planes are scheduling organizational units in the hardware layer 20, as shown in Figure 4A, where each context plane comprises logic elements LE.

Applicant respectfully requests that the Patent Office withdraw its rejection of claims 1-17 under 35 U.S.C. 112, second paragraph.

The Patent Office rejected claims 1 and 7 under 35 U.S.C. 102(e) as being anticipated by Karam, U.S. Patent No. 7,111,089.

A 37 C.F.R. 1.131 affidavit is being submitted with this response to overcome the effective filing date of December 23, 2002, U.S. Patent No. 7,111,089 to Karam. The attached exhibits A-D show that applicant conceived of the claimed invention no later than November 18, 2002, a date that precedes the effective filing date of Karam. Accordingly, Applicant respectfully requests that the Patent Office withdraw Karam as a prior art reference.

Furthermore, to show conception and diligence in the United States where the patent application was drafted, Exhibits A to B are provided (any redaction has been for the purpose of protecting confidential information):

1. Exhibit A is a true copy of a screen shot of the opened invention report document with the statistics windows of properties superimposed over a portion of the displayed document. This screen shot shows that the invention report for the invention entitled "Tiered Multi-media Acceleration Scheduler Architecture for dynamic configurable devices" by inventor Yoshiya Hirase was created on November 13, 2002, and last saved by inventor Hirase on November 18, 2002. Thus, conception occurred no later than November 13, 2002, and diligence has been shown through at least November 18, 2002.

2. Exhibit B is a true copy of the entire invention report referred to the paragraph immediately above.

3. Exhibit C is a true copy of an email dated December 13, 2002, by Applicant requesting that our firm prepare the present application (Applicant's docket number of NC39081US corresponds to U.S. patent application serial no. 10/740,034 and attorney docket no. 883.0006.U1(US)). This exhibit shows diligence on the part of Applicant and implies diligence on the part of the attorney as U.S. Provisional Patent Application No. 60/436,771, was filed thirteen days later on December 26, 2002.

4. The present application claims priority under 35 U.S.C. 119(e) from U.S. Provisional Patent Application No. 60/436,771, filed on December 26, 2002.

Conception is therefore shown prior to December 23 2002, and diligence is shown via the invention report created on November 13, 2002, and last saved November 18, 2002, the December 13, 2002, email requesting the firm of the undersigned attorney to file a U.S. provisional patent application for NC39081 (corresponding to the current patent application and U.S. Provisional Patent Application No. 60/436,771 from which it claims priority under 35 U.S.C. 119(e)), and the filing of U.S. Provisional Patent Application No. 60/436,771, on December 26, 2002.

All exhibits are true copies with the exception of being labeled herein for identification and redaction of confidential information.

Accordingly, Applicant requests that the Patent Office withdraw its rejection of claims 1 and 7 by Karam.

The Patent Office rejected claims 1-17 under 35 U.S.C. 103(a) as being unpatentable over Hoskins, U.S. Patent No. 6,789,132, in view of Kaihlaniemi, U.S. Patent No. 6,370,591.

Claim 1 recites as follows:

> A device architecture comprising: a processor arranged to run an operating system (OS) comprising an OS scheduler; hardware comprising a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs); and interposed between said OS and said DCHL layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) that cooperates with the OS scheduler for scheduling the LEs of the DCHL to execute applications in accordance with inherited application priorities.

Claim 7 recites as follows:

> A method comprising: providing an operating system (OS) comprising an OS scheduler and a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs); interposing between said OS and said DCHL layer a TiEred Multi-media Acceleration Scheduler (TEMAS); and operating the TEMAS in cooperation with the OS scheduler for scheduling the LEs of the DCHL to execute applications in accordance with inherited application priorities.

Claim 13 recites as follows:

> An apparatus comprising: an applications layer comprising a plurality of applications; a processor arranged to run a service layer comprising an operating system (OS) having an OS scheduler; hardware comprising a hardware layer comprising Dynamic Configurable Hardware Logic (DCHL) comprised of a plurality of Logic Elements (LEs); and interposed between said OS and said DCHL in said service layer and in a node layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) that cooperates with the OS scheduler for scheduling the LEs of the DCHL to execute said applications in accordance with inherited application priorities.

The Patent Office considers the scheduler module 222 to be the TiEred Multi-Media Acceleration Scheduler (TEMAS) and unit 110 and all of unit 202 except unit 222 to be the Dynamic Configurable Hardware Logic (DCHL), as shown in Figure 2 of Hoskins. The Patent Office asserted on page 6, lines 3-8, of the Office Action dated October 26 2007 as follows:

> a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs) (Fig 2, unit 110 and all of unit 202 except unit 222); and interposed between a host computer (Fig 2, unit 200) and said DCHL layer, a TiEred Multi-media Acceleration Scheduler (TEMAS) (Fig 2, unit 222) that cooperates with the host computer for scheduling and configuring the LEs of the DCHL to execute applications (Column 5, lines 35-39; Column 6, lines 1-10, lines 41-47).

Let us review the Patent Office's addressing of the claimed subject matter of the TEMAS that "cooperates with the OS scheduler for scheduling the LEs of the DCHL to execute applications in accordance with inherited application priorities." The Patent Office has asserted that the teachings are to be found in column 5, lines 35-39 and column 6, lines 1-10 and 41-47 of Hoskins.

Hoskins, column 5, lines 35-39, discloses "a host computer 200 is preferably operably

connected to a disc drive control module 202, such that data as well as control and interrupt commands may be received by the control module 202 from the host computer 200."

Hoskins, column 6, lines 1-10, discloses as follows:

> The control module 202 includes an interface module 204. The interface module 204 typically includes an associated buffer 208 which facilitates high speed data transfer between the host computer 200 and the disc drive 100. Data to be written to the disc drive 100 are passed from the host computer to the interface module 206 and then to a read/write channel module 210, which encodes and serializes the data and provides the requisite write current signals to the heads 118. To retrieve data that has been previously stored by the disc drive 100, read signals are generated by the heads 118 and provided to the read/write channel module 210

Hoskins, column 6, lines 41-47, discloses as follows:

> Central to the operation of the command module 220, and thus the disc drive, is the scheduler module 222, as shown in FIG. 3. The scheduler module 222 is employed in the disc drive 100 to schedule and dispatch the various modules of the command module 220 for processing by the processor module 212.

Figure 2 of Hoskins shows a functional block diagram of the disc drive 100 of Figure 1 comprising a host computer 200, a disc control module 202, and an actuator assembly 110 where the disc drive control module is operably connected to each of the host computer 200 and the actuator assembly 110. In the disc drive control module 202 are shown an interface module 204, a processor module 212, a spindle control module 216, a servo control module 218, a R/W channel module 210, and a command module 220. The interface module 204 is disclosed by Hoskins as facilitating high speed data transfer between the host computer 200 and disc drive 100 (column 6, lines 1-16), where data passes between the host computer 200 and the heads 118 via the interface module 204 and the read/write channel module 210.

Unit 222, the scheduler module 222 shown in Figure 2 of Hoskins, contrary to the Patent Office's assertions, is not disclosed as a TEMAS. TiEred Multi-media Acceleration Scheduler is described on page 5, lines 19-21, of Applicant's filed specification, as "a multi-layered scheduler, such as a two-layered scheduler." Hoskins does not disclose a multi-layer scheduler and, so, cannot disclose the claimed subject matter of a "TiEred Multi-media Acceleration Scheduler."

Kaihlaniemi discloses a communication module 10 that interfaces with an interfacing

application 7 and a supplementary driver 11 and another communication module 16 that interfaces with an interfacing application 8 and a supplementary driver 17. Kaihlaniemi does not remedy the above noted deficiency of Hoskins.

Furthermore, neither Hoskins nor Kaihlaniemi disclose "inherited application priorities."

Thus, any combination of these two references fails to make obvious any of claims 1-17, each of which recites "hardware comprising a Dynamic Configurable Hardware Logic (DCHL) layer comprised of a plurality of Logic Elements (LEs)" and "scheduling the LEs of the DCHL to execute said applications in accordance **with inherited application priorities**."

As such, claims 1-17 are allowable over Hoskins in view of Kaihlaniemi.

The Patent Office is respectfully requested to reconsider and remove the rejections of the claims 1-17 under double patent over claims 1-17 of U.S. Patent Application No. 10/740,034, claims 1-17 under 35 U.S.C. 112, second paragraph, claims 1 and 7 as being anticipated by Karam under 35 U.S.C. 102(e), and claims 1-17 as being unpatentable over Hoskins in view of Kaihlaniemi and to allow all of the pending claims 1-17 as now presented for examination. An early notification of the allowability of claims 1-17 is earnestly solicited.

Respectfully submitted:

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